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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,233	12/31/2001	Herve Cassagnes	01RO11554371	7300

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER

PHU, PHUONG M

ART UNIT PAPER NUMBER

2611

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/039,233

Applicant(s)

CASSAGNES, HERVE

Examiner

Phuong Phu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13,16-24,26-30 and 32-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13,16,18-20,22-24,26,27,29,30,32,33,35 is/are rejected.
- 7) ☒ Claim(s) 17,21,28 and 34 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 9/8/06. Accordingly, claims 13, 16-24, 26-30 and 32-35 are currently pending; and claims 1-12, 14, 15, 25 and 31 are canceled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "The decoding circuit of claim 15". It is unclear which decoding circuit that claim 16 refers to because claim 15 is a canceled claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13, 16, 19-20, 23, 24, 26, 27, 30, 32 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiramatsu (5,778,031), previously cited.

-Regarding to claims 13 and 30, see figures 5-7 and col. 4, line 34 to col. 8, line 24, Hiramatsu discloses a method and associated system (see figure 5) for decoding a biphasic signal comprising:

register step/means (31) of precharging the states (half bit data) “a0”, ..., “a5” of a biphasic signal (a), one state of the pair of states being precharged at each pulse of a periodic precharging signal (c) (see also figure 7); and

verification step/means (32-44) of comprising device (32), under operation “EXOR”, of comparing the two states of the pair of states to detect an error and providing an signal based upon detecting the error (see col. 6, lines 4-6) wherein the error comprises the two states being equal, e.g., providing a detection signal “1” based up on the detection of two states (a3) and (a4) being equal.

-Regarding to claim 32, Hiramatsu discloses that pair of states represent a value (see figure 6(a)), and wherein said verification also provides a decoded signal (Bi-PHASE SIGNAL DECODED OUTPUT) indicating the value of the precharged pair states (see figure 5).

-Regarding to claims 16 and 33, Hiramatsu discloses a storage circuit (12) (see figure 5) for storing the decoded signal at each pulse of a periodic validation signal (n), the periodic validation signal having a period equal to twice the period the periodic precharging signal (c) (see also figure 7).

-Claim 19 is rejected with similar reasons set forth for claim 13.

-Claim 20 is rejected with similar reasons set forth for claim 16.

-Claim 23 is rejected with similar reasons set forth for claim 13. Further regarding to claim 23, Hiramatsu discloses transmission and reception circuitry (figure 5) comprising a circuit (1) for sending biphasic signals to a receiving circuitry (circuits shown in figure 5 excluding circuit (1)).

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-Regarding to claim 24, Hiramatsu discloses that biphasic signals are encoded according to a protocol (see col. 1, lines 19-40).

-Claim 26 is rejected with similar reasons set forth for claim 15.

-Claim 27 is rejected with similar reasons set forth for claim 16.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 18, 22, 29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu in view of Okada et al (6,175,542), previously cited.

-Regarding to claims 18, 22, 29 and 35, Hiramatsu does not disclose that the biphasic signal is filtered prior to being precharged.

Okada et al teaches using a filter (98, 100) for filtering a received coded signal to be decoded so that noise in the received coded signal is reduced or eliminated by the filtering (see figures 7 and 12, and col. 8, lines 18-35).

It would have been obvious for one skilled in the art to implement in Hiramatsu invention a filter, as taught by Okada et al, in such a way that the filter would filter the biphasic signal from noise before the biphasic signal being precharged to be further decoded so that distortions, which are caused by the noise and may affect the performance of the decoding process, would be avoided.

Allowable Subject Matter

8. Claims 17, 21, 28 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments filed on 9/8/06 have been fully considered but they are not persuasive.

The applicant mainly argues that Hiramatsu does not teach procedure of detecting two states being equal constitute an error, as claimed.

The examiner respectfully disagrees. Note that the rejection based on the limitations recited in the claim. For instant, with respect to claim 1, the claim recites "A decoding circuit for decoding a biphasic signal having a pair of states and comprising a precharging register for precharging the states of the biphasic signal, one state of the of the pair of the states being precharged at each pulse of a periodic precharging signal; and a verification circuit for comparing the two states of the pair of states to detect an error and providing an error signal based upon detecting the error wherein the error comprises the two states being equal".

In comparison, Hiramatsu teaches a decoding circuit (see figure 5), as claimed, for decoding a biphasic signal (a) having a pair of states, e.g., a pair of states (a3, a4), the decoding circuit comprising:

a register device (31), (considered here equivalent with the limitation "precharging register"), of precharging the states (a3, a4) of the biphasic signal (a), one state of the pair of

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states (a3, a4) being precharged at each pulse of a periodic precharging signal (c) (see also (a), (b) and (c) of figure 7, c, col. 5, lines 38-40); and

verification circuit (32-44) which comprises device (32), under operation "EXOR", for comparing the two states (a3, a4) of the pair of states to detect a discrimination between the two states, (the discrimination considered here equivalent with the limitation "error"), and providing a detection signal, (considered here equivalent with the limitation "error signal"), based upon detecting the discrimination and providing the detection signal based up on the detection, e.g., providing a detection signal "1" if (a3) and (a4) are the same, wherein the discrimination comprises the two states (a3) and (a4) being equal (see col. 6, lines 3-6).

Therefore, it can be said here that Hiramatsu teaches procedure (32) of detecting two states being equal constitute an error, as claimed.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu

Phuong Phu
11/16/06

**PHUONG PHU
PRIMARY EXAMINER**

Phuong Phu
Primary Examiner
Art Unit 2611